Response Under 37 C.F.R.§1.116
Examining Group 2822
Expedited Procedure

Section I (Amendment to the Claims)

A listing of claims 1-32 of the present application, which are amended herein with markings to show changes made, is provided below:

1. (Currently amended) A structure for interconnecting semiconductor components comprising:

a layered substrate for transferring, said layered substrate is terminated with a terminal layer that includes at least one metallic component;

a bi-layer capping coating on top of the layered substrate, each layer of said coating provides adhesion and protection, said bi-layer capping coating comprising a first layer of silicon nitride entirely on said terminal layer including said at least one metallic ~~element~~ component and a second layer of an amino silane atop said first layer of ~~SiN~~ silicon nitride; and

a carrier assembly located atop said bi-layer capping coating.

2. (Previously presented) The structure according to claim 1 wherein said layered substrate contains at least one semiconductor component.

3. (Previously presented) The structure according to claim 2 wherein said at least one semiconductor component is selected from the group consisting of semiconductor devices, semiconductor circuits, thin-film layers, passive and/or active elements, interconnecting elements, memory elements, micro-electro-mechanical elements, optical elements, optoelectronic elements, and photonic elements.

4. (Original) The structure according to claim 1 wherein said carrier assembly comprises a carrier wafer, an adhesive layer and an intermediate layer.

5. (Original) The structure according to claim 1 wherein said carrier assembly comprises glass and an intermediate layer of polyimide.

6. (Original) The structure according to claim 4 wherein said carrier wafer is selected from the group consisting of silicon, silicon-on-insulator, silicon germanium-on-insulator, alumina, quartz, group III-V or II-VI semiconductor wafers, and ceramics.

7. (Cancelled).

8. (Previously presented) The structure according to claim 1 wherein said metallic component is a patterned wiring level or a blanket film.

9. (Previously presented) The structure according to claim 1 wherein said metallic component is selected from the group consisting Ti, Ta, Zr, Hf, their silicides nitrides and their conducting siliconitrides; Cu, Al, composites of these materials with glass; and combinations thereof.

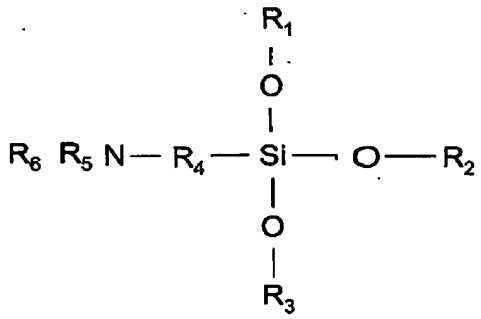
10. (Previously presented) The structure according to claim 1 wherein said capping coating provides passivation to the metallic component.

11. (Currently amended) The structure according to claim 1 wherein said ~~said~~ first layer serves as a diffusion barrier, while providing adhesion to the layered substrate; and said second layer provides adhesion to the carrier assembly and is an additional diffusion limiting layer.

12. (Cancelled).

13. (Previously presented) The structure according to claim 11 wherein said second layer is an adhesion promoter to an intermediate layer.

14. (Previously presented) The structure according to claim 1 wherein said amino silane is a compound of the formula:



wherein R_1, R_2, R_3, R_5 and R_6 are, independently of each other, hydrogen, a lower alkyl radical containing from 1 to about 6 carbon atoms, an acyl radical containing 1 to 6 carbon atoms, or an allyl, alkylene or alkynyl radical containing 2 to 6 carbon atoms, and R_4 is a lower alkyl containing from 1 to 6 carbon atoms or an aromatic system.

15. (Original) The structure according to claim 5 wherein said polyimide material is selected from the group consisting of polyamic acid (PAA)-based polyimides, polyimic ester-based polyimides, and pre-imidized polyimides.

16. (Previously presented) The structure according to claim 5 wherein said carrier assembly comprises glass and an intermediate layer of polyimide to allow for a further release process.

17. (Original) The structure according to claim 11 wherein said first layer further serves as protection against a removal process of said carrier assembly.

18. (Original) The structure according to claim 17 wherein said first layer protects from an oxygen-based plasma removal process.

19. (Withdrawn) A method of constructing a structure for interconnecting semiconductor components, comprising the steps of

providing a substrate to be transferred;

forming a bi-layer capping coating on the substrate, each layer of said capping coating providing protection and adhesion; and

forming a carrier assembly on the capping coating.

20. (Withdrawn) The method of claim 19 wherein said carrier assembly is formed by:
applying an adhesive coating on a top of a carrier wafer; and
depositing an intermediate layer on the adhesive coating.

21. (Withdrawn) The method of claim 19 wherein said capping coating is formed by depositing at least two consecutive layers and hence creating a bi-layer protecting said substrate to be transferred from negative effects of attachment and the later removal processes of said carrier assembly.

22. (Withdrawn) The method of claim 19 wherein said bi-layer capping is formed by:
forming a first layer of the bi-layer capping coating for providing a barrier to diffusion and adhesion to said substrate to be transferred; and
forming a second layer of bi-layer capping coating for providing adhesion to said carrier assembly and providing further protection against diffusion.

23. (Withdrawn) The method of claim 19 wherein bi-layer capping coating is formed by spin on coating, plasma enhanced deposition, physical or chemical vapor deposition.

24. (Withdrawn) A method for wafer-level layer transfer comprising the steps of:
providing a layer to be transferred on a semiconductor substrate;
forming a first layer of a capping coating on said layer to be transferred, said first layer provides adhesion and protection from oxidation;
forming a second layer of the capping coating on said first layer, said second layer provides additional protection and adhesion to a carrier assembly;
adhering said carrier assembly to a carrier wafer by bonding; and
removing said semiconductor substrate such that said layer to be transferred is attached to said carrier assembly thereby achieving layer transfer.

25. (Withdrawn) The method according to claim 24, further comprising the steps of joining an exposed surface of said transferred layer to a top surface of a receiver substrate, removing said carrier assembly to achieve further transfer of said transferred layer from said carrier assembly to said receiver substrate.

26. (Withdrawn) The method according to claim 25, wherein said semiconductor and receiver substrates contain semiconductor components and said carrier assembly is used to enable the layer transfer of said semiconductor components from the semiconductor substrate on to the semiconductor components from the receiver substrate.

27. (Withdrawn) The method according to claim 26, wherein the semiconductor and receiver substrates are selected from the group consisting of silicon, silicon on insulator, II-VI compounds, III-V compounds, alumina and quartz.

28. (Withdrawn) The method according to claim 26, wherein said semiconducting components are selected from the group comprising of semiconductor devices, semiconductor circuits, thin-film layers, passive and active elements, interconnecting elements, memory elements, micro-electro- mechanical elements, optical elements, optoelectronic elements, and photonic elements.

29. (Withdrawn) The method according to claim 24, wherein the material of said carrier wafer is selected from glass and quartz.

30. (Withdrawn) The method according to claim 24, wherein said carrier wafer adheres to an intermediate layer made of polyimide.

31. (Withdrawn) The method according to claim 30, wherein said release process of said carrier wafer is based on a laser ablation process where polyimide absorbs all the energy allowing for separation of a wafer carrier from the structure.

32. (Withdrawn) The method of 24 wherein the steps are repeated numerous times to provide a multi-level three-dimensional structure.